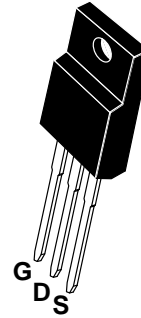


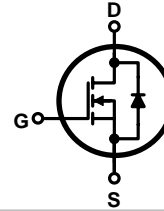


**Features**

- 18A, 650V, RDS(on) = 380mΩ @VGS = 10 V
- Low gate charge ( typical 38nC)
- Low Crss ( typical 6.2pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



Schematic diagram



Marking Diagram



- Y = Year
- A = Assembly Location
- WW = Work Week
- VT = Version & Thickness
- FIR18N65F = Specific Device Code

**General Description**

This Power MOSFET is produced by HSDQ using its own advanced planar stripe DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology.

Symbol	Parameter	Value	Units
V <sub>DSS</sub>	Drain-Source Voltage	650	V
I <sub>D</sub>	Drain Current - Continuous (TC= 25°C)	18	A
	- Continuous (TC= 100°C)	11.7*	A
I <sub>DM</sub>	Drain Current - Pulsed (Note 1)	72*	A
V <sub>GSS</sub>	Gate-Source Voltage	± 30	V
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Note 2)	340	mJ
I <sub>AR</sub>	Avalanche Current (Note 1)	18	A
E <sub>AR</sub>	Repetitive Avalanche Energy (Note 1)	48	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	5	V/ns
P <sub>D</sub>	Power Dissipation (TC = 25°C)	35.0	W
	- Derate above 25°C	0.28	W/°C
T <sub>j</sub> , T <sub>stg</sub>	Operating and Storage Temperature Range	-55 to +150	°C
T <sub>L</sub>	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	°C

\* Drain current limited by maximum junction temperature

**Thermal Characteristics**

Symbol	Parameter	Value	Units
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case	3.55	°C/W
R <sub>θJS</sub>	Thermal Resistance, Case-to-Sink Typ.	--	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient	43.2	°C/W



Electrical Characteristics <small>TC = 25°C unless otherwise noted</small>						
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	650			V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to 25°C		0.61		V/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 670\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 400\text{ V}, TC = 125^\circ\text{C}$			10	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$			100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$			-100	nA
<b>On Characteristics</b>						
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D =250\ \mu\text{A}$	3.0		5.0	V
$R_{DS(On)}$	Drain-Source On-state Resistance	$V_{GS}=10\text{ V}, I_D =9\text{ A}, T_J = 25^\circ\text{C}$		380	480	m $\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 9\text{ A}$ (Note 4)		17		S
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$		2150		pF
$C_{oss}$	Output Capacitance			265		pF
$C_{rss}$	Reverse Transfer Capacitance			6.2		pF
<b>Switching Characteristics</b>						
$t_{d(on)}$	Turn On Delay Time	$V_{DD} = 335\text{ V}, I_D = 18\text{ A}, R_G = 25\ \Omega$ (Note 4, 5)		36		ns
$t_r$	Rising Time			51		ns
$t_{d(off)}$	Turn Off Delay Time			80		ns
$t_f$	Fall Time			44		ns
$Q_g$	Total Gate Charge	$V_{DS} = 335\text{ V}, I_D = 18\text{ A}, V_{GS} = 10\text{ V}$ (Note 4, 5)		38		nC
$Q_{gs}$	Gate-Source Charge			12		nC
$Q_{gd}$	Gate-Drain Charge			13		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
$I_S$	Maximum Continuous Drain-Source Diode Forward Current				18	A
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current				72	A
$V_{SD}$	Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 18\text{ A}$			1.4	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 18\text{ A}, di_F / dt = 100\text{ A}/\mu\text{s}$		456		ns
$Q_{rr}$	Reverse Recovery Charge	Note 4)		5.9		$\mu\text{C}$
<b>Notes:</b> 1. Repetitive Rating : Pulse width limited by maximum junction temperature 2. $L = 2.1\text{ mH}, I_{AS} = 18\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega$ , Starting $T_J = 25^\circ\text{C}$ 3. $I_{SD} \leq 20\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , Starting $T_J = 25^\circ\text{C}$ 4. Pulse Test : Pulse width $\leq 300\ \mu\text{s}$ , Duty cycle $\leq 2\%$ 5. Essentially independent of operating temperature						



### Typical Characteristics

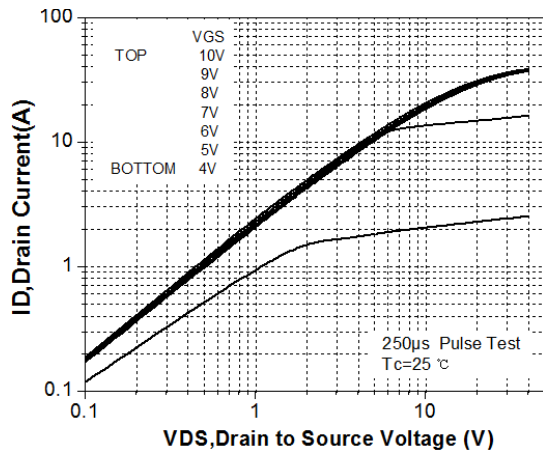


Figure 1. On-Region Characteristics

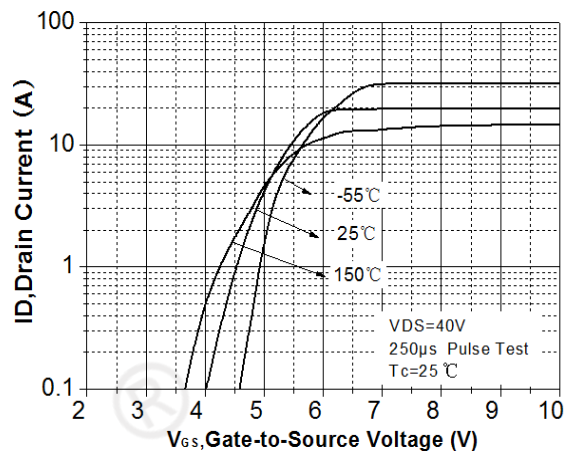


Figure 2. Transfer Characteristics

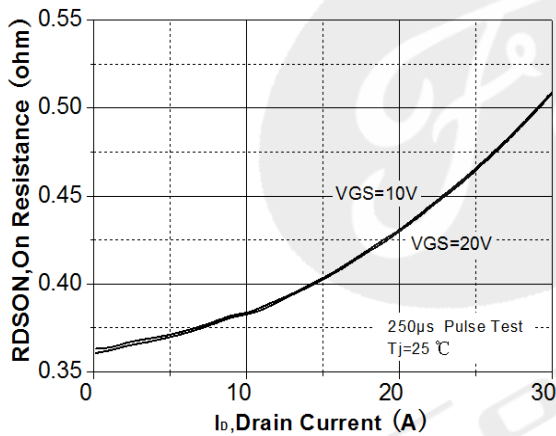


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

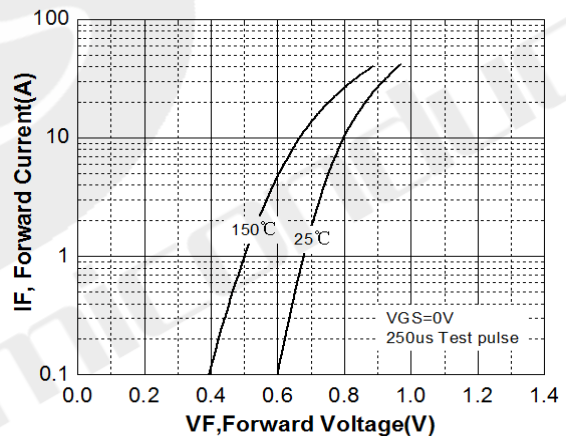


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

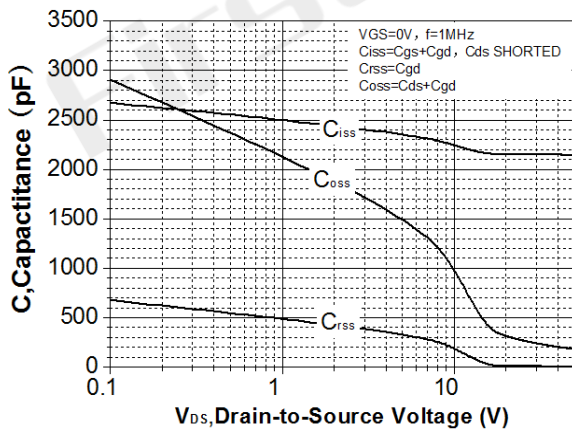


Figure 5. Capacitance Characteristics

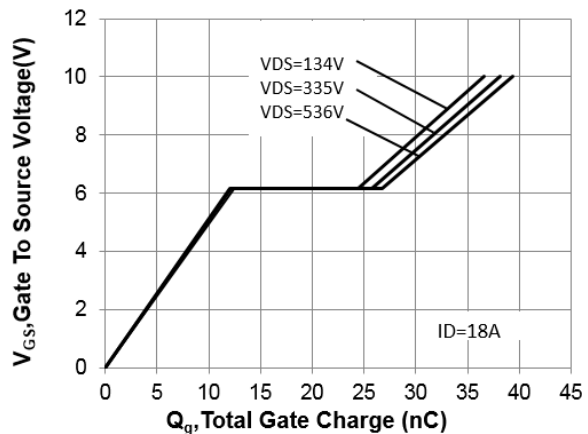


Figure 6. Gate Charge Characteristics



Typical Characteristics (Continued)

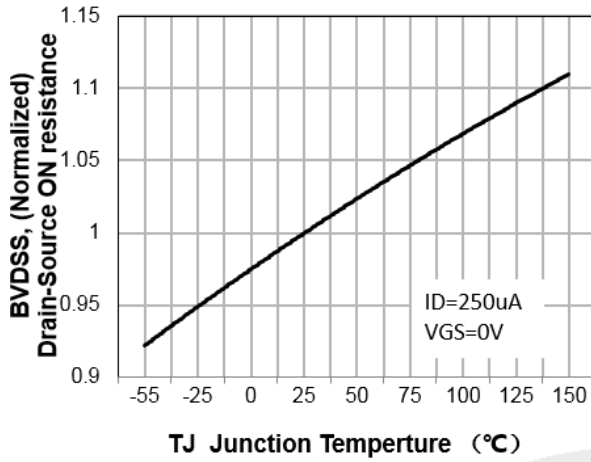


Figure 7. Breakdown Voltage Variation vs Temperature

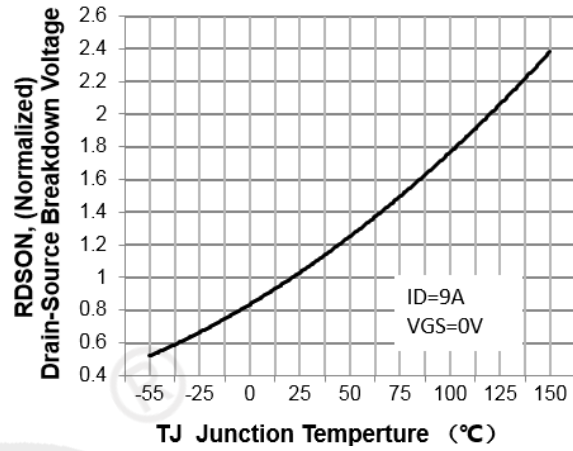


Figure 8. On-Resistance Variation vs Temperature

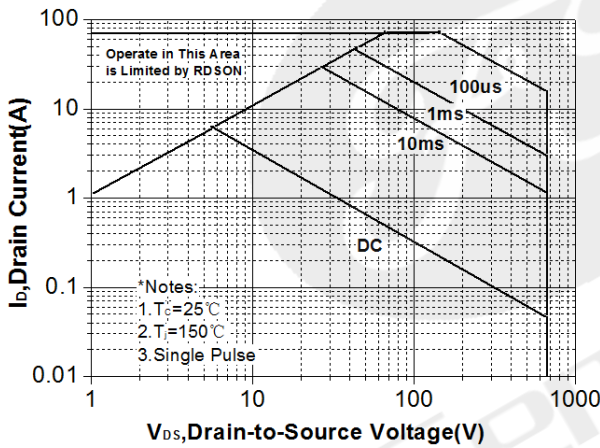


Figure 9. Maximum Safe Operating Area

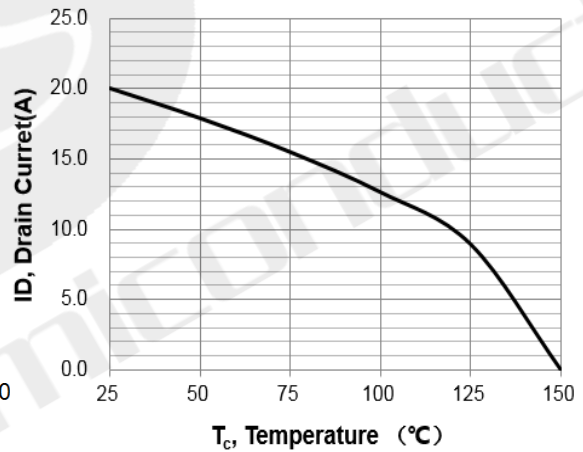


Figure 10. Maximum Drain Current vs Case Temperature

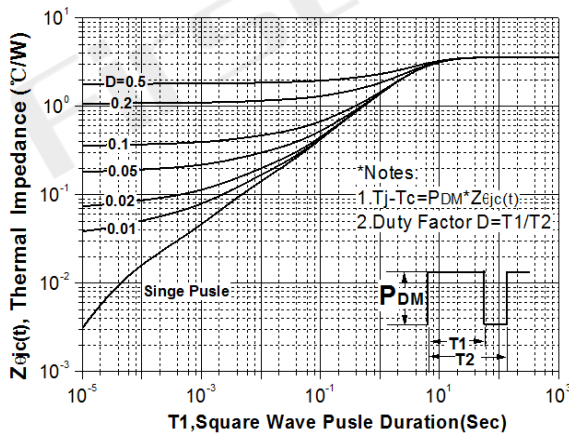
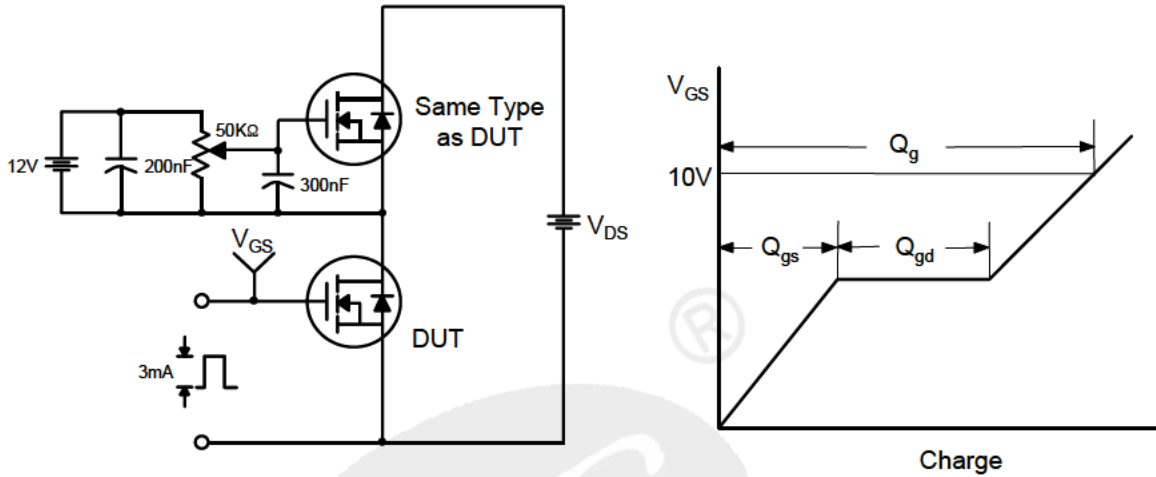
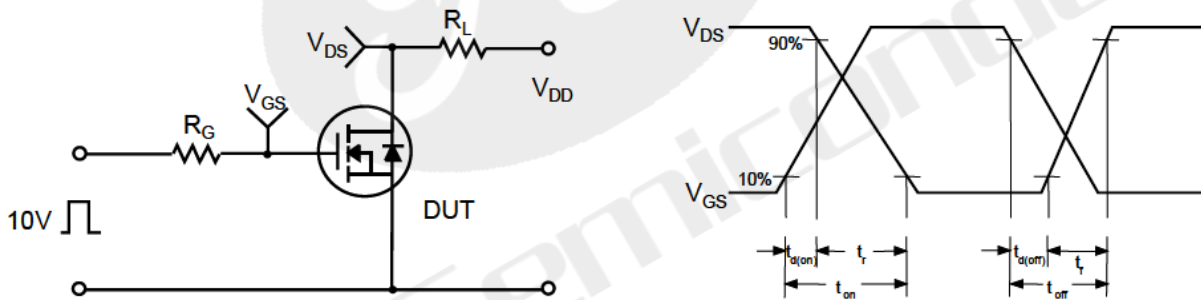


Figure 11. Transient Thermal Response Curve

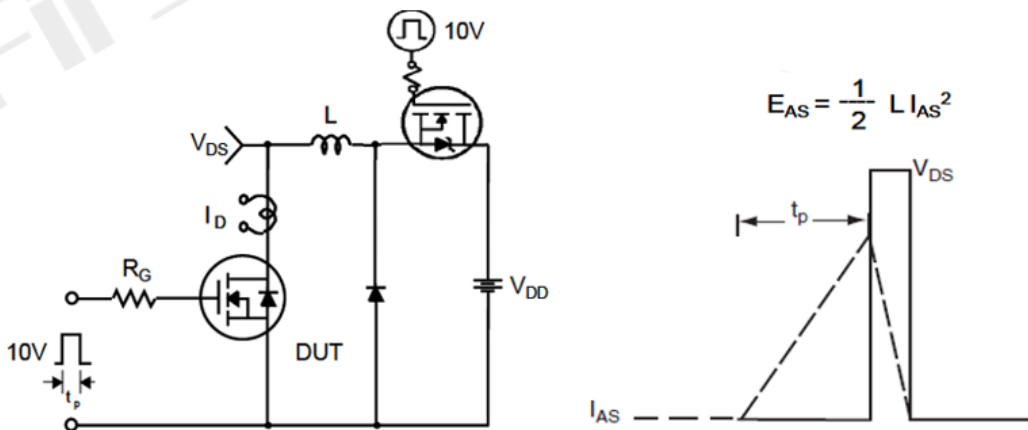
Gate Charge Test Circuit & Waveform



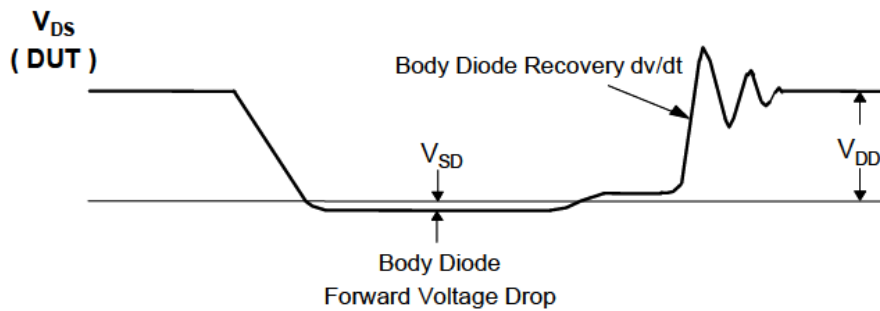
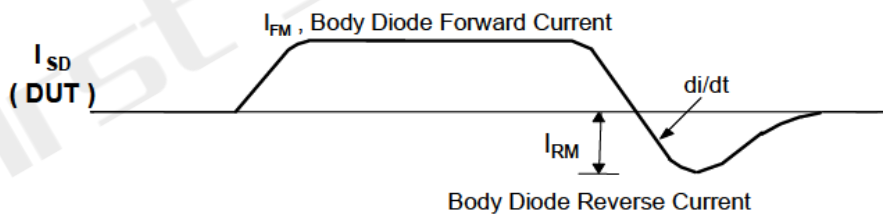
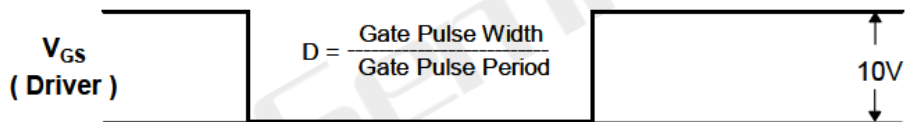
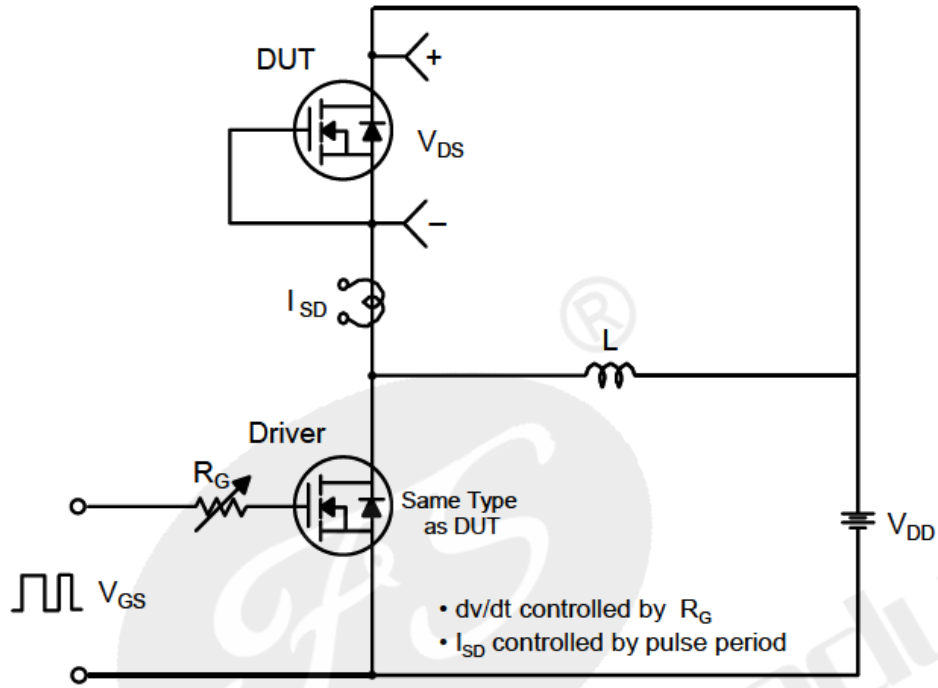
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms



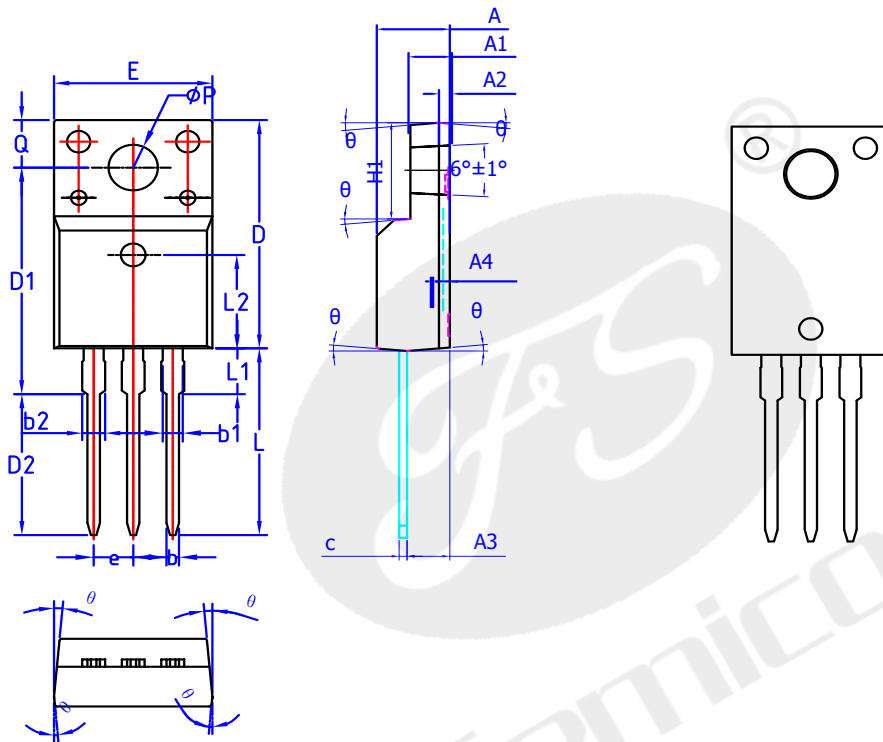
Peak Diode Recovery dv/dt Test Circuit & Waveforms





Package Information

TO-220F



Units: mm  
COMMON DIMENSIONS  
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	4.50	4.70	4.90
A1	2.34	2.54	2.74
A2	0.70 REF		
A3	2.56	2.76	2.96
b	0.70	0.80	0.90
b1	1.17	1.2	1.25
b2	1.17	1.2	1.25
c	0.45	0.50	0.60
D	15.67	15.87	16.07
D1	15.55	15.75	15.95
D2	10.0	10.2	10.4
E	9.96	10.16	10.36
e	2.54BSC		
H1	6.48	6.68	6.88
L	12.68	12.98	13.28
L1	-	-	3.50
L2	6.50REF		
ØP	3.08	3.18	3.28
Q	3.20	3.30	3.40
θ 1	1°	3°	5°
A4	0.53	0.56	0.59



Declaration

- FIRST reserves the right to change the specifications, the same specifications of products due to different packaging line mold, the size of the appearance will be slightly different, shipped in kind, without notice! Customers should obtain the latest version information before ordering, and verify whether the relevant information is complete and up-to-date.
- Any semiconductor product under certain conditions has the possibility of failure or failure, The buyer has the responsibility to comply with safety standards and take safety measures when using FIRST products for system design and manufacturing, To avoid To avoid potential failure risks, which may cause personal injury or property damage!
- Product promotion endless, our company will wholeheartedly provide customers with better products!

**ATTACHMENT**

Revision History

Date	REV	Description	Page
2019.01.01	1.0	Initial release	